MSC 4604
LSI-11 DUAL-HIGH MEMORY SYSTEM

M4604

14 Inverness Drive East
Englewood, Colorado, 80112
(303) 770-7400

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305-0225-000	P.C. BOARD SCHEMATIC

SECTION 1

INTRODUCTION

1.1 SCOPE

This manual provides information that the user needs to understand and maintain the MSC 4606 -- a semiconductor memory system that fulfills LSI-11 bus protocol.

1.2 UNIT DESCRIPTION

The MSC 4604 is a single-board, dual-high memory system that is compatible with the LSI-11 Q-BUS*. Organization of the MSC 4604 is based on a 16K X 1 NMOS dynamic RAM. These elements mount on a 8.5- by 5.2-inch printed-circuit board along with the necessary interface components to configure up to 589,824 bits of storage capacity on one board.

Voltage normally present on the LSI-11 backplane supply the power required by the MSC 4604. An on-board DC-to-DC converter uses +12V line to generate the -5V substrate bias for the NMOS storage elements.

1.3 CONFIGURATION

Four major configurations of the MSC 4604 are available. They are: (1) 16K X 16, (2) 32K X 16, (3) 16K X 18, and (4) 32K X 18. Modular addressing is switch selectable. The starting address can be set to any 1K boundaries from 0 to 128K. Furthermore, the board capacity is on 1K boundaries so that the user can use 1K, 2K or 3K of the I/O page for main memory.

*LSI-11 and Q-Bus are Digital Equipment Corp. Trademarks.

1.3.1 Battery Back Up

Uninterruptable voltage sources may be connected to the MSC 4604 via the Q-BUS, which will power only the array and refresh logic. In this mode, non-volitility can be maintained during power failures and/or extended power down. This option is jumper selectable on the MSC 4604.

1.3.2 Refresh

The MSC 4604 has the capability to perform three modes of refresh operation. These switch selectable options include internal distributed refresh, and external refresh with or without the generation of the reply signal that is asserted to the bus master.

SECTION 2

SPECIFICATIONS

2.1 SCOPE

This section presents specifications and capabilities of the MSC 4604.

2.2 SPECIFICATIONS

2.2.1 Access/Cycle Time

Access (nanoseconds):

	Typical	Maximum
Read (DATI)	240	255
Write (DATO)	240	255
Read-Modify-Write	665	685

Cycle (nanoseconds):

	Typical	Maximum
Q-BUS	SYNC H + 20	SYNC H + 32
Refresh (including arbritration)	540	580

Assumptions: SYNC H to DIN H - 25 nanoseconds
SYNC H to DOUT H - 50 nanoseconds
RPLY H to DOUT H - 350 nanoseconds

2.2.2 Power Requirements

DC Requirements: LSI-11 backplane supplies require DC voltages See Table 2-1 for power requirements of each configuration.

ORGANIZATION	BATTERY BACKUP	SUPPLY VOLTAGE	OPERATING CURRENT(A)		STANDBY CURRENT(A)		POWERED DOWN CURRENT	
			Typ.	Max.	Typ.	Max.	Typ.	Max.
32K X 18	YES	+5V	0.54	0.80	0.46	0.68	-	-
		+5VB	0.76	1.10	0.72	1.05	0.76	1.10
		+12VB	0.34	0.48	0.06	0.10	0.12	0.17
16K X 18	YES	+5V	4.54	0.80	0.40	0.68	-	-
		+5VB	0.76	1.10	0.72	1.05	0.76	1.10
		+12VB	0.25	0.40	0.04	0.08	0.07	0.11
32K X 16	YES	+5V	0.54	0.80	0.46	0.68	-	-
		+5VB	0.76	1.10	0.72	1.05	0.76	1.10
		+12VB	0.34	0.48	0.06	0.10	0.12	0.17
16K X 16	YES	+5V	0.54	0.80	0.46	0.68	-	-
		+5VB	0.76	1.10	0.72	1.05	0.76	1.10
		12VB	0.25	0.40	0.04	0.08	0.12	0.11
32K X 18	NO	+5V	1.30	1.90	1.18	1.73	-	-
		+12V	0.34	0.48	0.06	0.10	-	-
16K X 18	NO	+5V	1.30	0.90	1.73	1.73	-	-
		+12V	0.25	0.40	0.04	0.08	-	-
32K X 16	NO	+5V	1.30	1.90	1.18	1.73	-	-
		+12V	0.34	0.48	0.06	0.10	-	-
16K X 16	NO	+5V	1.30	0.90	1.73	1.73	-	-
		+12V	0.25	0.40	0.04	0.08	-	-

Table 2-1
MSC 4604 POWER REQUIREMENTS

2.2.3 Bus Signals

All logic levels to and from the bus are TTL compatible. All Q-BUS timing conforms to LSI-11 protocol. I/O pin assignments of the MSC 4604 are listed in Table 2-2.

BUS PIN	A CONNECTOR		B CONNECTOR	
	SIDE 1	SIDE 2	SIDE 1	SIDE 2
A	-	+5V	BDCOK H	+5V
B	-	-	-	-
C	BDAL16L	GND	-	GND
D	BDAL17L	+12V	-	+12V
E	-	BDOUTL	-	BDAL02L
F	-	BRPLYL	-	BDAL03L
H	-	BDINL	-	BDAL04L
J	GND	BSYNL	GND	BDAL05L
K	REFKILL	BWTBTL	-	BDAL06L
L	-	-	-	BDAL07L
M	GND	BIAKIL	GND	BDAL08L
N	-	BIAKOL	-	BDAL09L
P	-	-	-	BDAL10L
R	BREFL	BDMGIL	-	BDAL11L
S	+12B	BDMGOL	-	BDAL12L
T	GND	-	GND	BDAL13L
U	-	BDAL00L	-	BDAL14L
V	+5V	BDAL01L	+5V	BDAL15L

Table 2-2
MSC 4604 I/O CONFIGURATION

2.2.4 Bus Load

AC Load: The MSC 4604 presents two AC loads to the bus (18.7 pF of capacitance maximum).

DC Load: The MSC 4604 presents one DC load to the bus (105 microamperes of leakage current nominal)

2.2.5 Operating Environments

Operating Temperature:	0° C to +50° C
Storage Temperature:	-40° C to +66° C
Relative Humidity:	up to 90% without condensation

2.2.6 Physical Dimensions

Mounted on a glass-epoxy, printed-circuit board with the following dimensions:

Height: 5.2 in. (13.2 cm).
Length: 8.5 in. (21.6 cm).
Non-conductive component height limit: 0.375 in. (0.97 cm) max.

2.3 CAPABILITIES

2.3.1 Address Channel

The MSC 4604 accepts 18 bits of address information that locates a unique data word. Address bits BDAL01 L thru BDAL17 L select the memory location, and BDAL00 L denotes the byte. The incoming address is latched into an address register upon the initiation of BSYNC L.

2.3.1.1 Address Programming

On-board DIP switches allow the user to quickly change the starting address and storage capacity of the MSC 4604 in 1K increments. The incoming address lines are compared with the programmed switch settings. In event the address is within the programmed limits, the designated memory operation is then initiated.

2.3.2 Data Channel

Data is transferred to, or received from, the bus master on Q-BUS lines BDAL00 L thru BDAL15 L during the DIN or DOUT portions of the bus cycle.

2.3.3 LSI-11 Bus Interface

The MSC 4604 meets Digital Equipment Corporation specifications protocol for the LSI-11 Bus. Two signals achieve synchronization between the processor and the MSC 4604 -- BSYNC L (Bus Sync) and BRPLY L (Bus Reply). The bus master asserts BSYNC L to initiate a cycle and indicate that address information is present on the bus. The master then asserts BDIN L for a read or BDOUT L for a write operation. The MSC 4604 acknowledges with BRPLY L to indicate to the master that either data is available (read command) or data has been accepted from the bus (write command) respectively.

2.3.3.1 Data Transfer Cycles

When data is read out of an addressed memory location, this is called a DATI bus cycle. If data is transferred from the bus to the addressed location, this is a DATO cycle or write operation. In addition, DATIO cycles indicate an output transfer succeeding an input transfer. This cycle provides an efficient means of executing a read-modify-write operation by making it unnecessary to assert an address a second time (IN and OUT designations are bus master references).

2.3.3.2 DATIO Cycle

A DATIO cycle is equivalent to a read-modify-write operation. An addressing operation and an input word transfer are first executed as described in paragraphs 4.3.2 (DATI). However, BSYNC L remains in an active state after the input data transfer is complete. This causes the MSC 4604 to remain selected, and an output data transfer follows without further addressing. After completing the output data transfer operation, the DATIO cycle is complete when BSYNC L is unasserted.

2.3.3.3 Refresh

Refresh of the dynamic storage cell requires that each of the row addresses be asserted within two milliseconds. This requires a minimum of 128 refresh cycles every two milliseconds. When neither a write nor read operation is in progress, a refresh cycle may be initiated. If a read or write is asserted on the bus during a refresh cycle, the Q-BUS information is stored until the refresh cycle is complete.

The MSC 4604 controls all refresh functions and timing as required for internal distributed refresh. For external refresh, the bus master asserts BREF L during the address portion of each refresh cycle for each BSYNC/BDIN operation. BREF L allows all dynamic memory elements of the MSC 4604 to be enabled and addressed simultaneously.

During external refresh operation, only the slowest device being refreshed should generate a reply. Whether or not the MSC 4604 responds with BRPLY L is switch selectable.

2.3.4 Timing And Control

Delay-line circuitry establishes the internal timing as required for proper operation of the MSC 4604. For external control, the MSC 4604 accepts LSI-11 bus signals. Table 2-3 lists and describes these signals.

MNEMONIC	DESCRIPTION	FUNCTION
BDAL0 L-BDAL17 L	Data Address Bits	Transfer Address and data information between the MSC 4604 and the bus master. The bus master asserts the address data on the bus first, and then the MSC 4604 either receives or sends the data word on the same lines.
BSYNC L	Bus Sync	Generate by the bus master to initiate a cycle and indicate that the address is on BDAL0 L thru BDAL17 L. The requested transfer remains in process until SYNC L is negated.
BDIN L	Data In	Involved with two bus operations. When asserted by the bus master during BSYNC L, the master device is ready to accept data from the MSC 4604. An interrupt operation is indicated when BDIL L is asserted with out BSYNC L.
BDOUT L	Data Output	Implies valid data is available on the bus and that an output transfer with respect to the bus master, is taking place. The MSC 4604 responds to BDOUT L with BRPLY L to complete the transfer.
BRPLY L	Reply	Is asserted by the MSC 4604 in response to either BDOUT L or BDIN L.

Table 2-3
BUS CONTROL SIGNALS.

MNEMONIC	DESCRIPTION	FUNCTION
BWTBT L	Write/Byte	Controls the MSC 4604 two ways. If asserted during the leading edge of BSYNC L, an output sequence (DATO or DATOB) will follow. If unasserted during the leading adge of BSYNC L, a DATI or DATIO cycle will follow. BWTBT L is also asserted during BDOUT L in a DATOB bus cycle to indicate byte addressing.
BREF L	Memory Refresh	When asserted by a bus master, activates all NMOS memory elements for each BSYNC L/BDIN L transaction.
REFKIL L	Refresh Control	Inhibits internal refresh cycles.

Table 2-3(cont.)
BUS CONTROL SIGNALS

SECTION 3

INSTALLATION

3.1 SCOPE

This section gives recommended procedures for properly installing the MSC 4604.

3.2 UNPACKING AND INSPECTION

Carefully remove the memory system from the shipping container and packing material from the assembly. Inspect the board for damage or loose connections and components.

3.3 INSTALLATION

After the initial inspection, use the step-by-step procedure that is outlined in the following paragraphs for system installation.

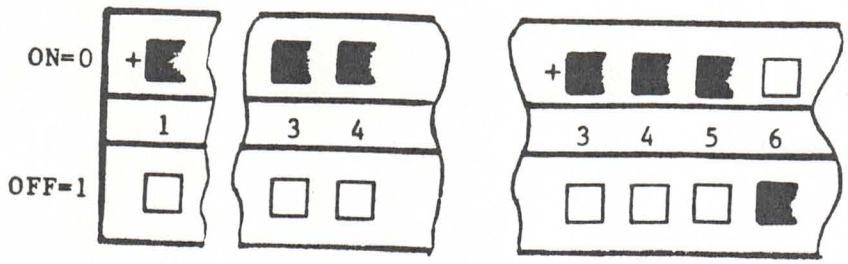
1) Set up the on-board DIP switches SW1 and SW2 using Table 3-1 (starting address) and 3-2 (capacity). The following example demonstrates how to program these switches.

EXAMPLE 3-1: PROGRAMMING THE ADDRESS SWITCHES

For a 32K system with a starting address of 8K, the switch settings are determined in the following manner:

A. STARTING ADDRESS

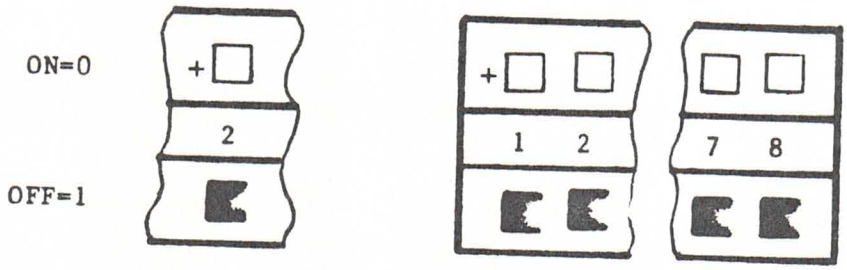
Using Table 3-1, 8K setting of SW1 and SW2 is illustrated in the following diagram (shaded area indicates the switch is depressed to that side).



SW2 SW1

B. CAPACITY

The following diagram illustrates the DIP switch setting for 32K capacity using Table 3-2 (shaded area indicates the switch is depressed to that side).



SW2 SW1

STARTING ADDRESS		SWITCH SETTING							STARTING ADDRESS		SWITCH SETTING						
		SW2			SW1						SW2			SW1			
K	OCTAL	3	4	1	6	3	4	5	K	OCTAL	3	4	1	6	3	4	5
0	000000	0	0	0	0	0	0	0	32	200000	0	1	0	0	0	0	0
1	004000	0	0	0	0	0	0	1	33	204000	0	1	0	0	0	0	1
2	010000	0	0	0	0	0	1	0	34	210000	0	1	0	0	0	1	0
3	014000	0	0	0	0	0	1	1	35	214000	0	1	0	0	0	1	1
4	020000	0	0	0	0	1	0	0	36	220000	0	1	0	0	1	0	0
5	024000	0	0	0	0	1	0	1	37	224000	0	1	0	0	1	0	1
6	030000	0	0	0	0	1	1	0	38	230000	0	1	0	0	1	1	0
7	034000	0	0	0	0	1	1	1	39	234000	0	1	0	0	1	1	1
8	040000	0	0	0	1	0	0	0	40	240000	0	1	0	1	0	0	0
9	044000	0	0	0	1	0	0	1	41	244000	0	1	0	1	0	0	1
10	050000	0	0	0	1	0	1	0	42	250000	0	1	0	1	0	1	0
11	054000	0	0	0	1	0	1	1	43	254000	0	1	0	1	0	1	1
12	060000	0	0	0	1	1	0	0	44	260000	0	1	0	1	1	0	0
13	064000	0	0	0	1	1	0	1	45	264000	0	1	0	1	1	0	1
14	070000	0	0	0	1	1	1	0	46	270000	0	1	0	1	1	1	0
15	074000	0	0	0	1	1	1	1	47	274000	0	1	0	1	1	1	1
16	100000	0	0	1	0	0	0	0	48	300000	0	1	1	0	0	0	0
17	104000	0	0	1	0	0	0	1	49	304000	0	1	1	0	0	0	1
18	110000	0	0	1	0	0	1	0	50	310000	0	1	1	0	0	1	0
19	114000	0	0	1	0	0	1	1	51	314000	0	1	1	0	0	1	1
20	120000	0	0	1	0	1	0	0	52	320000	0	1	1	0	1	0	0
21	124000	0	0	1	0	1	0	1	53	324000	0	1	1	0	1	0	1
22	130000	0	0	1	0	1	1	0	54	330000	0	1	1	0	1	1	0
23	134000	0	0	1	0	1	1	1	55	334000	0	1	1	0	1	1	1
24	140000	0	0	1	1	0	0	0	56	340000	0	1	1	1	0	0	0
25	144000	0	0	1	1	0	0	1	57	344000	0	1	1	1	0	0	1
26	150000	0	0	1	1	0	1	0	58	350000	0	1	1	1	0	1	0
27	154000	0	0	1	1	0	1	1	59	354000	0	1	1	1	0	1	1
28	160000	0	0	1	1	1	0	0	60	360000	0	1	1	1	1	0	0
29	164000	0	0	1	1	1	0	1	61	364000	0	1	1	1	1	0	1
30	170000	0	0	1	1	1	1	0	62	370000	0	1	1	1	1	1	0
31	174000	0	0	1	1	1	1	1	63	374000	0	1	1	1	1	1	1

(0=ON, 1=OFF)

Table 3-1
STARTING ADDRESS SWITCH SETTINGS

STARTING ADDRESS		SWITCH SETTING							STARTING ADDRESS		SWITCH SETTING						
		SW2			SW1						SW2			SW1			
K	OCTAL	3	4	1	6	3	4	5	K	OCTAL	3	4	1	6	3	4	5
64	400000	1	0	0	0	0	0	0	96	600000	1	1	0	0	0	0	0
65	404000	1	0	0	0	0	0	1	97	604000	1	1	0	0	0	0	1
66	410000	1	0	0	0	0	1	0	98	610000	1	1	0	0	0	1	0
67	414000	1	0	0	0	0	1	1	100	614000	1	1	0	0	0	1	1
68	420000	1	0	0	0	1	0	0	101	620000	1	1	0	0	1	0	0
69	424000	1	0	0	0	1	0	1	102	624000	1	1	0	0	1	0	1
70	430000	1	0	0	0	1	1	0	103	630000	1	1	0	0	1	1	0
71	434000	1	0	0	0	1	1	1	104	634000	1	1	0	0	1	1	1
72	440000	1	0	0	1	0	0	0	105	640000	1	1	0	1	0	0	0
73	444000	1	0	0	1	0	0	1	106	644000	1	1	0	1	0	0	1
74	450000	1	0	0	1	0	1	0	107	650000	1	1	0	1	0	1	0
75	454000	1	0	0	1	0	1	1	108	654000	1	1	0	1	0	1	1
76	460000	1	0	0	1	1	0	0	109	660000	1	1	0	1	1	0	0
77	464000	1	0	0	1	1	0	1	110	664000	1	1	0	1	1	0	1
78	470000	1	0	0	1	1	1	0	111	670000	1	1	0	1	1	1	0
79	474000	1	0	0	1	1	1	1	112	674000	1	1	0	1	1	1	1
80	500000	1	0	1	0	0	0	0	113	700000	1	1	1	0	0	0	0
81	504000	1	0	1	0	0	0	1	114	704000	1	1	1	0	0	0	1
82	510000	1	0	1	0	0	1	0	115	710000	1	1	1	0	0	1	0
83	514000	1	0	1	0	0	1	1	116	714000	1	1	1	0	0	1	1
84	520000	1	0	1	0	1	0	0	117	720000	1	1	1	0	1	0	0
85	524000	1	0	1	0	1	0	1	118	724000	1	1	1	0	1	0	1
86	530000	1	0	1	0	1	1	0	119	730000	1	1	1	0	1	1	0
87	534000	1	0	1	0	1	1	1	120	734000	1	1	1	0	1	1	1
88	540000	1	0	1	1	0	0	0	121	740000	1	1	1	1	0	0	0
89	544000	1	0	1	1	0	0	1	122	744000	1	1	1	1	0	0	1
90	550000	1	0	1	1	0	1	0	123	750000	1	1	1	1	0	1	0
91	554000	1	0	1	1	0	1	1	124	754000	1	1	1	1	0	1	1
92	560000	1	0	1	1	1	0	0	125	760000	1	1	1	1	1	0	0
93	564000	1	0	1	1	1	0	1	126	764000	1	1	1	1	1	0	1
94	570000	1	0	1	1	1	1	0	127	770000	1	1	1	1	1	1	0
95	574000	1	0	1	1	1	1	1	128	774000	1	1	1	1	1	1	1

(0=ON, 1=OFF)

Table 3-1 (cont.)
STARTING ADDRESS SWITCH SETTINGS

MEMORY SIZE (K)	SWITCH SETTINGS					
	SW2	SW1				
	2	8	1	2	7	
1	0	0	0	0	0	
2	0	0	0	0	1	
3	0	0	0	1	0	
4	0	0	0	1	1	
5	0	0	1	0	0	
6	0	0	1	0	1	
7	0	0	1	1	0	
8	0	0	1	1	1	
9	0	1	0	0	0	
10	0	1	0	0	1	
11	0	1	0	1	0	
12	0	1	0	1	1	
13	0	1	1	0	0	
14	0	1	1	0	1	
15	0	1	1	1	0	
16	0	1	1	1	1	
17	1	0	0	0	0	
18	1	0	0	0	1	
19	1	0	0	1	0	
20	1	0	0	1	1	
21	1	0	1	0	0	
22	1	0	1	0	1	
23	1	0	1	1	0	
24	1	0	1	1	1	
25	1	1	0	0	0	
26	1	1	0	0	1	
27	1	1	0	1	0	
28	1	1	0	1	1	
29	1	1	1	0	0	
30	1	1	1	0	1	
31	1	1	1	1	0	
32	1	1	1	1	1	

(0=ON, 1=OFF)

Table 3-2
SWITCH SETTING FOR CAPACITY

SECTION 4

THEORY OF OPERATION

4.1 SCOPE

This section details the theory of operation that is necessary to understand and maintain the MSC 4604.

4.2 SYSTEM INTERFACE

The MSC 4604 interfaces with the LSI-11 bus via standard DEC block. For signal and pin identification, see Table 2-2.

4.3 SYSTEM DESCRIPTION

The MSC 4604 performs either a read or write operation using the LSI-11 bus signals listed in Table 2-2.

4.3.1 Address

The MSC 4604 processes the 16-bit address on input lines BDAL0 thru BDAL15 in the following manner:

1) When the bus master places the address on BDAL0 L thru BDAL15 L and asserts BSYNC L, the MSC 4604 determines if the memory is to be accessed. These address lines, routed through the bus receivers are compared with the setting of on-board DIP switches. The procedure for setting up these switches is outlined in paragraph 3.3.

2) If it is established on the leading edge of BYSNC L that the MSC 4604 is accessible, the address field is latched and decoded to select a unique memory location. Also, the requested memory operation as defined by either BDIN L or BDOUT L is initiated. Whenever the requested bus cycle is DATOB, signal BDAL00 L defines the byte that is to be modified during the write operation.

4.3.2 Read (DATI)

The DATI cycle transfers data from the MSC 4604 to the LSI-11 bus. If a DATI cycle is requested, the MSC 4604 responds in the following manner:

1) The bus master asserts the address information on BDAL00 L thru BDAL15 L. After 150 nanoseconds, the bus master then asserts BYSNC L.

2) The MSC 4604 accepts the address information. Upon receipt of BYSNC L, the address is then latched and decoded if the address presented is within the programmed limits.

3) The bus master removes the address from BDAL00 L thru BDAL15 L and asserts BDIN L.

4) When the data read from the addressed location becomes stable, this information is then asserted onto the bus. To indicate that data is now available, the MSC 4604 sends BRPLY L to the bus master. If BRPLY L is not asserted within 10 microseconds (maximum) after BDIN L is asserted, the bus master terminates the cycle and goes into a trap routine (Timeout).

5) The bus master clears BDIN L to acknowledge receipt of the data. In turn, the MSC 4604 negates BRPLY L. The cycle is complete when the bus master clears BSYNC L. The system is now ready for another transaction.

4.3.3 Write (DATO or DATOB)

Both DATO and DATOB involve data transfers from the bus master to the MSC 4604. The only difference is that DATO signifies a word transfer and DATOB is a byte transfer. The following functions are performed during the write cycle:

1) The bus master asserts the address information BDAL00 L thru BDAL15 L and BWTBT L. After 150 nanoseconds, the bus master then asserts BSYNC L.

2) The MSC 4604 accepts the address, and then compares the address information with the programmed address limits. If the address data is valid, the board is enabled upon receipt of BSYNC L.

3) The bus master removes the address from BDAL00 L thru BDAL15 L and negates BWTBT L. Following a short time delay, the data word is placed on the bus (BDAL00 L thru BDAL15 L). In turn, BDOUT L is asserted to signify that valid data is now available on the bus.

4) The MSC 4604 accepts the information on the data line BDAL00 L thru BDAL15 L. In response to the BDOUT L signal, the MSC 4604 asserts BRPLY L to complete the transfer. If BRPLY L is not asserted within 10 microseconds, the bus master terminates the cycle (Timeout).

5) The bus master responds to BRPLY L by clearing BDOUT L, and BWTBT L if the requested transfer cycle is DATOB.

6) The MSC 4604 negates BRPLY L to release the bus for another transaction while completing internal write functions. In turn, the bus master clears BYSNC L to finish the cycle and prepare for the next operation.

4.4.1 Memory Addressing

Transceivers accept the address word on bus input lines BDAL00 L thru BDAL17 L, and convert them to internal signals A00 thru A17. Adders U2 and U12 assign the starting address for the MSC 4604 as "ADDRESS 0", based on the settings of SW1 and SW2, and the summation outputs of U2 and U12 to establish the storage capacity. The carry output or pin 14 of U3 remains "high" as long as the address word accepted from the bus is within the programmed limits of the MSC 4604. In turn, a "low" signifies that the programmed capacity has been exceeded and all requested memory operations will be inhibited (pin 4, U14).

4.4.2 Address Decoding

When the requested memory operation is initiated, the "low" that is asserted on BSYNC L loads the row address and column address in tri-state latches U6 and U5 respectively. Under control of EN RAS ADD L (row select) and EN CAS ADD L (column select), address bits A00 thru thru A06 (row address) are multiplexed with address bits A07 thru A15 (column address) to be used as required by the memory elements. Signal BSYNC L also latches address bits A15 thru A17 in U4.

4.4.2.1 Refresh Address

The outputs of tri-state driver U7 are multiplexed with row/column address bits A01 thru A15. When there is no memory operation in progress, pins 1 and 19 of U7 go "low", asserting the outputs of the Refresh counter U14 onto the row/column select lines. As the Refresh counter is incremented following each refresh cycle, the address applied to the memory elements changes accordingly.

4.4.3 Data Path

The MSC 4604 routes 16-bits of data (BDAL00 L thru BDAL15 L) to and from the bus for either a read or write operation via transceivers U8, 9, 30 and 32. If a write operation is requested, signal DOUT H (BDOUT L inverted) allows the data word to flow from the bus through U30 and U32. Under control of DIN L or DOUT L, transceivers U8 and U9 then convert BDAL00 L thru BDAL15 L to internal signals DI00 thru DI15. In turn, the resultant signals are applied to the selected memory array location and stored.

4.4.4 Timing And Control

The timing and control circuits perform two functions: (1) decode the command signals that are asserted on the bus, and (2) generate the control signals and timing sequence as required to perform the designated memory operation.

4.4.4.1 Read Command

For a read command, the "low" asserted on BSYNC L enables the condition of the carry line from adder U3 (See paragraph 4.4.1) in U35. If the address is within the programmed limits, a "high" is placed on pin 1 of U24. This signal in conjunction with SYN H (BYSNC L inverted) conditions flip-flop U35. In turn, this forces MEM CY H "high" (U35, pin 9), and a "low" is then placed on the input of the delay line U20 (DLA).

BDIN L causes EN and DLB (tap 1 of U27) to generate RPLY H (U20, pin 5) via gates U11 and U26. Drive U39 then asserts this signal as BRPLY L onto the bus. This timing operation allows the data word to read out of the memory and be placed onto the bus under control of DIR H.

4.4.4.2 Write Command

Generation of MEM CY H and the delay-line timing is the same as previously described in paragraph 4.4.4.1. However, DIN L remains "high" causing DIR H to remain "low", (U19, pin 6) and the bus transceivers to accept and transfer the data word from the Q-BUS onto the internal data bus DA01 L In turn, the "low" on DIR H also allows EN CAS ADD L o transfer this data into the addressed location via U8 and U10.

Signal WTBT H with A00 L (BDAL00 L) designates byte or word operation. If WTBT H is "low", both pins 12 and 13 of U17 will be "high", applying a "low" on both WE or Write Enable lines (U9, pins 2 and 5) to the memory chips -- causing the complete word to be written into memory. A "high" on WTBT H defines a write operation on byte basis (DATOB). Now pins 12 and 13 of U17 are conditioned (high) so that the state of A00 L controls which WE line will go "low" through the decoding gates of U17.

4.4.4.3 Internal Timing And Control

As the "low" and "high" levels shift through delay lines DLA (U26) and DLB (U27), the output taps are encoded to provide the timing pulses as required by both the memory elements and the MSC 4604. Each delay line has five delay taps with a 50-nanosecond delay between taps.

The normal quiescent state for DLA is "high" and for DLB is "low". The setting of U21 (MEM CY H) forces pin 12 of U35 "high". If a refresh cycle is not in progress (REF CY H). the "high" on input pin 12 of U35 applies a "low" on the input of DLA. This "low" then traverses through DLA. Signal DLA3 is applied to U35, pin 2 and U25, pin 1. Gate U35 (pins 1 thru 3) enables DOUT OR DIN H to set CAS EN H "high" (U21, pin 5). This "high" (CAS EN H) is asserted also on the input of DLB> Tap 1 of DLB generates BRPLY L which resets DIN OR DOUT H. This then sends a "low" a through DLB, and BRPLY L is reset. When BRPLY L goes "high", BSYNC L is then unasserted on the bus; EN MEM L (U14, pin 6) goes "high"; and latch U35 is reset, forcing MEM CY H "low". In turn, the inputs of DLA goes "high", which is shifted through the delay line U26.

4.4.4.4 Refresh Cycle

Refresh of the dynamic storage cell requires that each of the row addresses to be cycled within two-milliseconds. This requires a minimum of 128 cycles every two-milliseconds. Timer U24 controls this timing requirement. This timer is set up to generate a pulse width of 11- to 13-milliseconds on pin 4, allowing 128 cycles to be completed well within the two-millisecond requirement. Upon timing out, pin 4 of U24 goes "high", requesting a refresh cycle through U25, pins 11 thru 13.

If neither a read or write has been requested (pin 8 of U21 is "high"), the 100 nanosecond pulse on pin 12 of U24 sets the Refresh latch U40 (a "high" on pin 9), forcing REF CY H "high". This "high" indicates a refresh cycle has been initiated. The action of the Refresh latch inhibits CAS L circuits so that all chips are inhibited from performing a normal memory cycle. The Refresh counter U15 is incremented when a refresh cycle terminates. Encoding the signals from taps 3 and 4 of DLA generates RST REF H, which asserts a "low" on pin 13 of U40. This action forces pin 9 of U40 "low" and timer U24 is then retriggered. Upon timing out (pin 4 goes "low"), the 100 nanosecond pulse on pin 12 of U24 initiates a refresh cycle through the setting of the Refresh latch U40.

4.4.4.5 Refresh Kill

This signal provides a means for halting internal refresh cycles at a specific time. When REF KILL L is asserted, any refresh in progress is allowed to terminate, but succeeding cycles are disabled -- terminating any further refresh cycles.

4.4.4.6 External Refresh

An external source may be used to initiate a refresh cycle through the assertion of bus signal BREF L. This signal may be asserted during the address time for a single-cycle refresh, or held "low" for burst (repeated) refresh cycles. Bus receiver U38 accepts and generates the internal signal REF H. This signal (REF H) clocks the Refresh latch U40, initiating the refresh cycle.

When RST REF H goes "high" (Refer to paragraph 4.4.4.4), Refresh latch U40 is reset. The resultant "low" on pin 9 of U40 clocks Refresh Latch 2 (U40, pin 3), forcing ST REF 2L (pin 6) "high". This action places a "high" on pin 10 of U24 and allows DLA1 to trigger U24, pin 12. After 100 nanoseconds, U24 times out and the signal change on pin 12 clocks the Refresh latch, starting a second refresh cycle.

An open condition of SW3 (pins 4 and 6) disables RPLY H to allow the slowest device on the bus to send a reply. When the switch SW3 is closed, the MSC 4604 asserts BRPLY L onto the Q-BUS.

4.4.4.7 Parity

The MSC 4604 can check parity bits on a byte basis, expanding the data word from 16 to 18 bits -- one parity bit per byte. During a memory operation, parity circuits U16 (Byte 1) and U8 (Byte 0) checks the data word for correct parity. A "low" signal on BDAL16 L during the assertion of BRPLY L on the Q-BUS signifies a parity error.

SECTION 5

PREVENTIVE MAINTENANCE/TROUBLESHOOTING

5.1 SCOPE

This section describes the procedure that is recommended for troubleshooting the MSC 4604. The procedures that are outlined in this section are based on the fact that the user understands the normal operation of the MSC 4604 as described in the previous sections of this manual.

5.2 MAINTENANCE

Due to the solid-state nature of this memory system, maintenance requirements are minimum. However, running a memory diagnostic periodically guarentees memory integrity.

5.3 TROUBLESHOOTING

If a diagnostic or some other test indicates that the memory board is defective, check all voltages first. Then verify the presence of all bus signals.

Address lines should be confirmed in conjunction with the data input signals. If the board is functional except for a bit error at a specific address, then the defective element may be located using Drawing 305-0225-000 with Section 4 as a reference. If the board is determined to be defective, and a faulty element cannot be located or replaced, call the factory.

SECTION 6

WARRANTY

6.1 SCOPE

Monolithic Systems Corporation (MSC) warrants for a period of twelve (12) months from the data of shipment that each item of equipment (except those materials supplied by Buyer) shall be free from defects in material and workmanship under normal use and service. Any equipment which is not as warranted may be returned to Monolithic Systems Corporation at MSC's risk and expense for repair or replacement.

If the Buyer establishes that anyone of the items of equipment is not as warranted above in order to benefit from the warranty, the Buyer shall advise Monolithic Systems Corporation in writing during the warranty period describing in detail the defect claimed. Monolithic Sytems Corporation shall thereafter be afforded the opportunity, for a reasonable period of time after the defective equipment is returned to Monolithic Systems Corporation place of manufacture, to modify, adjust or repair such item of equipment in order to render it in conformity with the above warranty. If at the end of such period, the Buyer establishes that such item of equipment is still not in conformity with the above warrant then Monolithic Systems Corporation shall replace the defective item of equipment to the Buyer. The Buyer recognizes that the remedy of refund of the purchase price in the case of the breach by Monolithic Systems Corporation of the above warranty constitutes the sole and exclusive remedy to the Buyer for such breach. Equipment may consist of whole or in part, of refurbished components which are warranted equivalent to new when used for the purposes intended.

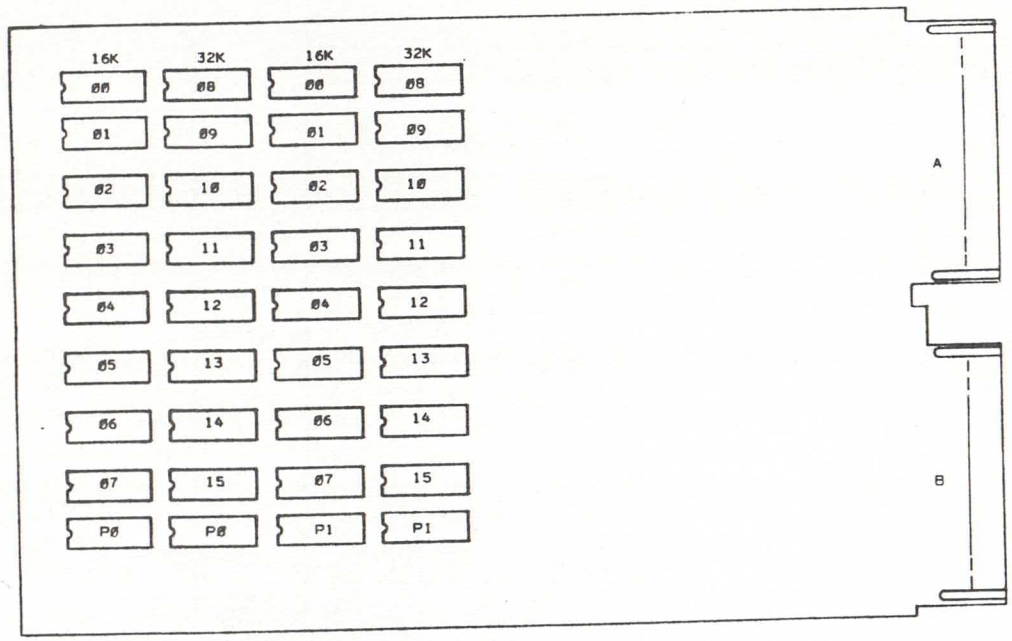
This warranty shall immediately terminate if the equipment is subjected to misuse, neglect, accident, damage in transit, transported in other than Monolithic Systems Corporation authorized containers, or is altered, repaired or overhauled by any person other than Monolithic Systems Corporation.

THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, PROMISES, AFFIRMATIONS OR REPRESENTATIONS, WHATSOEVER, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR IMPLIED WARRANTY OF FITNESS OF EQUIPMENT FOR A PARTICULAR PURPOSE, AND OF ANY OTHER OBLIGATIONS ON THE PART OF THE SELLER.

6.2 WARRANTY REGISTRATION

To expedite our warranty service, please fill out the WARRANTY REGISTRATION card at the front of this manual, and return to Monolithic Systems Corporation.

REVISIONS				
LTR	ECO	DESCRIPTION	DATE	APPRV'D
B	2133	ENGINEERING RELEASE	5/31/80	[illegible]



5. SEE PARTS LIST FOR OPTIONAL PARTS. (Q3, U8, U10, U32, U33).

4. REFERENCE 303-0225-000, SHEET 5, FOR MEMORY ELEMENT REFERENCE DESIGNATIONS PER DESIRED DASH NUMBER CONFIGURATION.

3. REFERENCE DESIGNATIONS:

LAST USED:						NOT USED
—	—	Q3	T1	—	—	—
C63	—	R5	—	—	—	
CR2	L1	RN18	U40	U136	—	U41-U100
E6	—	—	—	—	—	—
—	—	SW3	—	—	—	—

2. ASTERISK (*) INDICATES BATTERY BACK-UP.

1. ALL RESISTANCES IN OHMS, 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND ARE AFTER PLATING
TOLERANCES ON DECIMALS
FRACTIONS ± | .X ± | XX ± | XXX ± | ANGLES ±
MATERIAL

REV	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9

REVISION STATUS OF SHEETS

DRAWN	[illegible]	3-7-79
CHECKED	[illegible]	2-15-80
APPROVED		
APPROVED		

MONOLITHIC SYSTEMS CORP.
Englewood, Colorado 80112

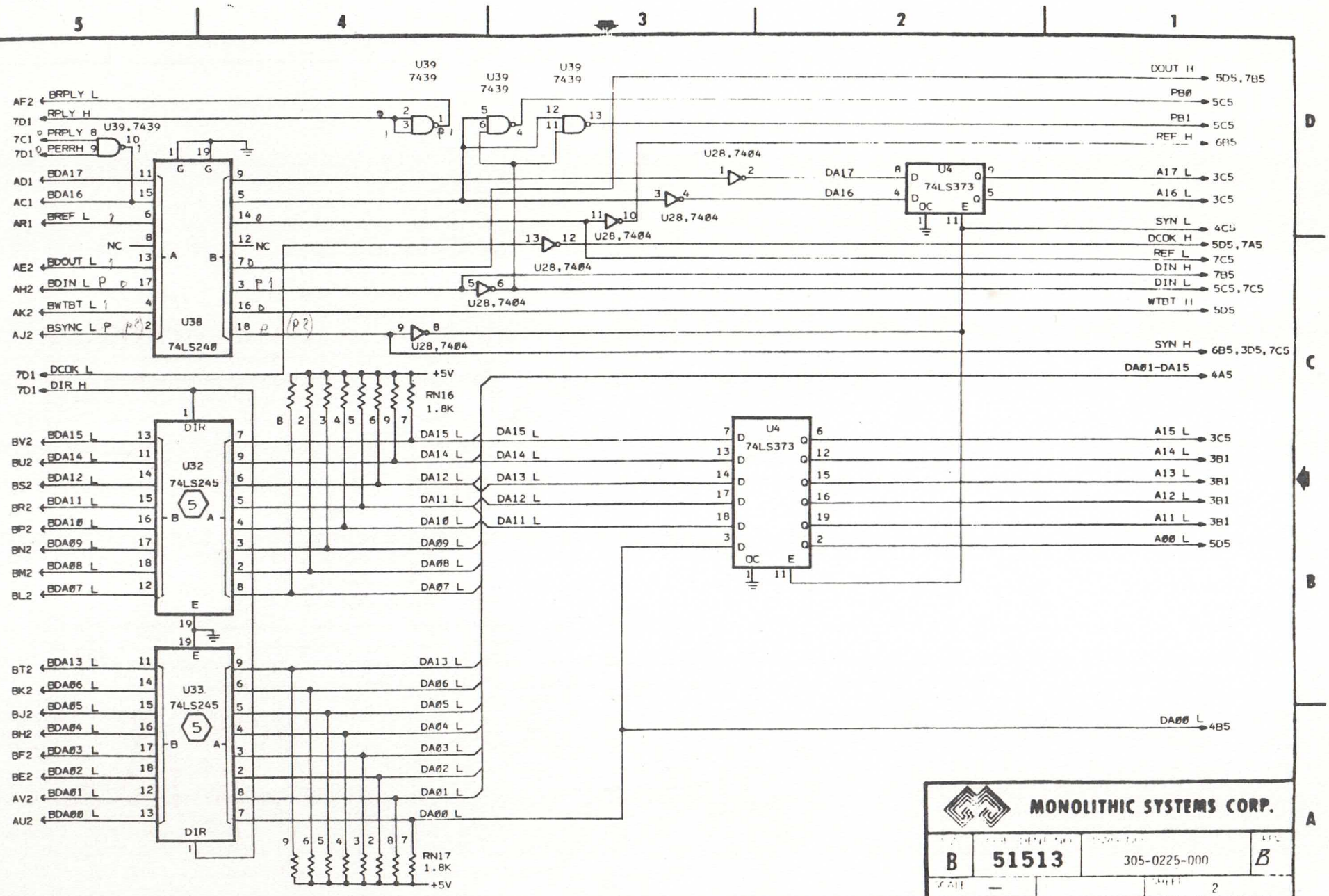
TITLE: P.C.B. SCHEMATIC
LSI-11, MSC 4604/4504

DWG REV: B

SIZE: B | CODE IDENT NO.: 51513 | DWG NO.: 305-0225-000

SCALE: 1/1 | SHEET 1 of 9

MSF 1052


U39 7439
U28,7404
U4 74LS373
U38 74LS240
U32 74LS245
U33 74LS245
RN16 1.8K
RN17 1.8K
+5V
BRPLY L
RPLY H
PRPLY B
PERRH
BDA17
BDA16
BREF L
BDOUT L
BDIN L
BWTBT L
BSYNC L
DCOK L
DIR H
BDA15 L
BDA14 L
BDA12 L
BDA11 L
BDA10 L
BDA09 L
BDA08 L
BDA07 L
BDA13 L
BDA06 L
BDA05 L
BDA04 L
BDA03 L
BDA02 L
BDA01 L
BDA00 L
DOUT H
PB0
PB1
REF H
A17 L
A16 L
SYN L
DCOK H
REF L
DIN H
DIN L
WTBT H
SYN H
DA01-DA15
A15 L
A14 L
A13 L
A12 L
A11 L
A00 L
DA00 L
MONOLITHIC SYSTEMS CORP.
51513
305-0225-000
B
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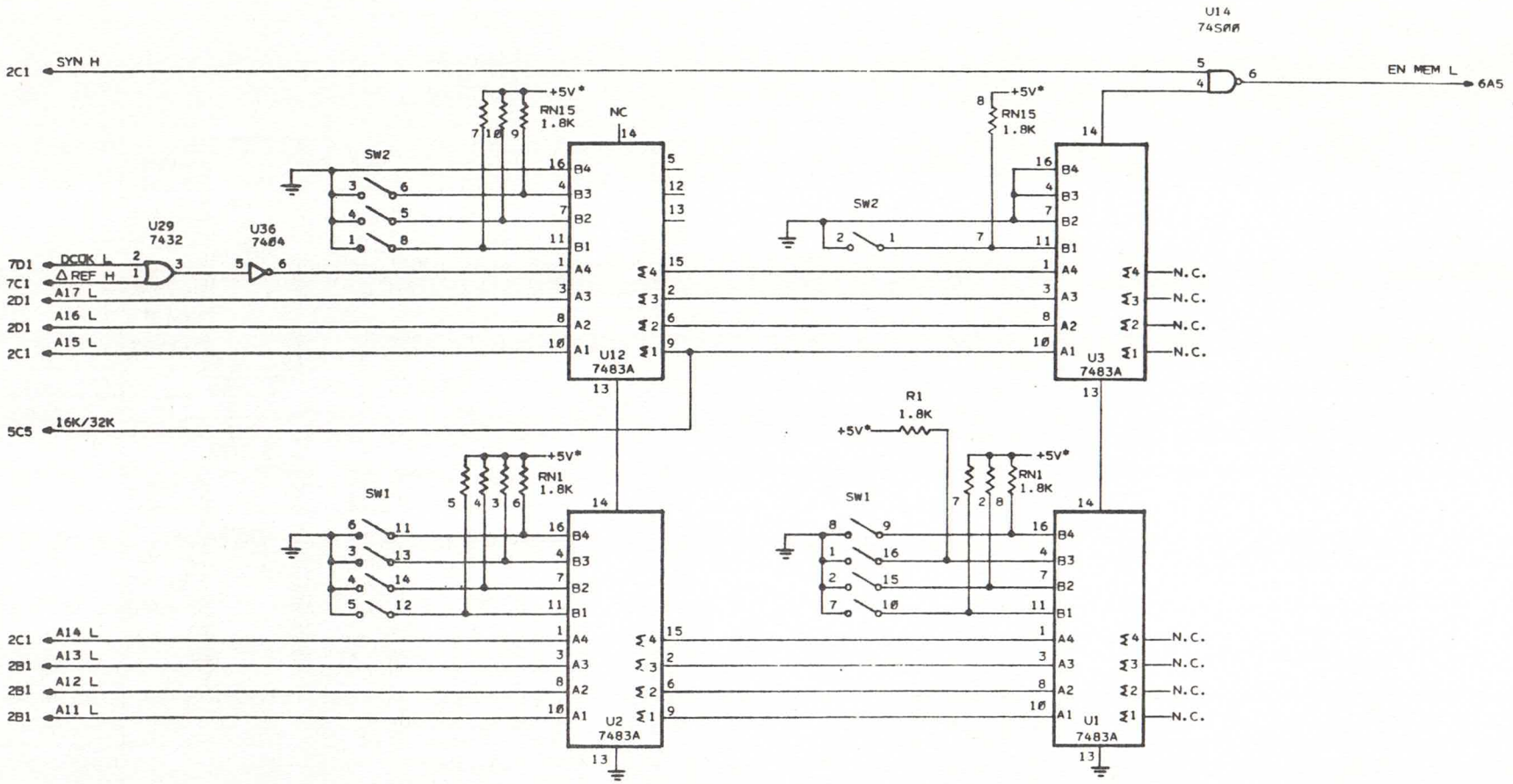

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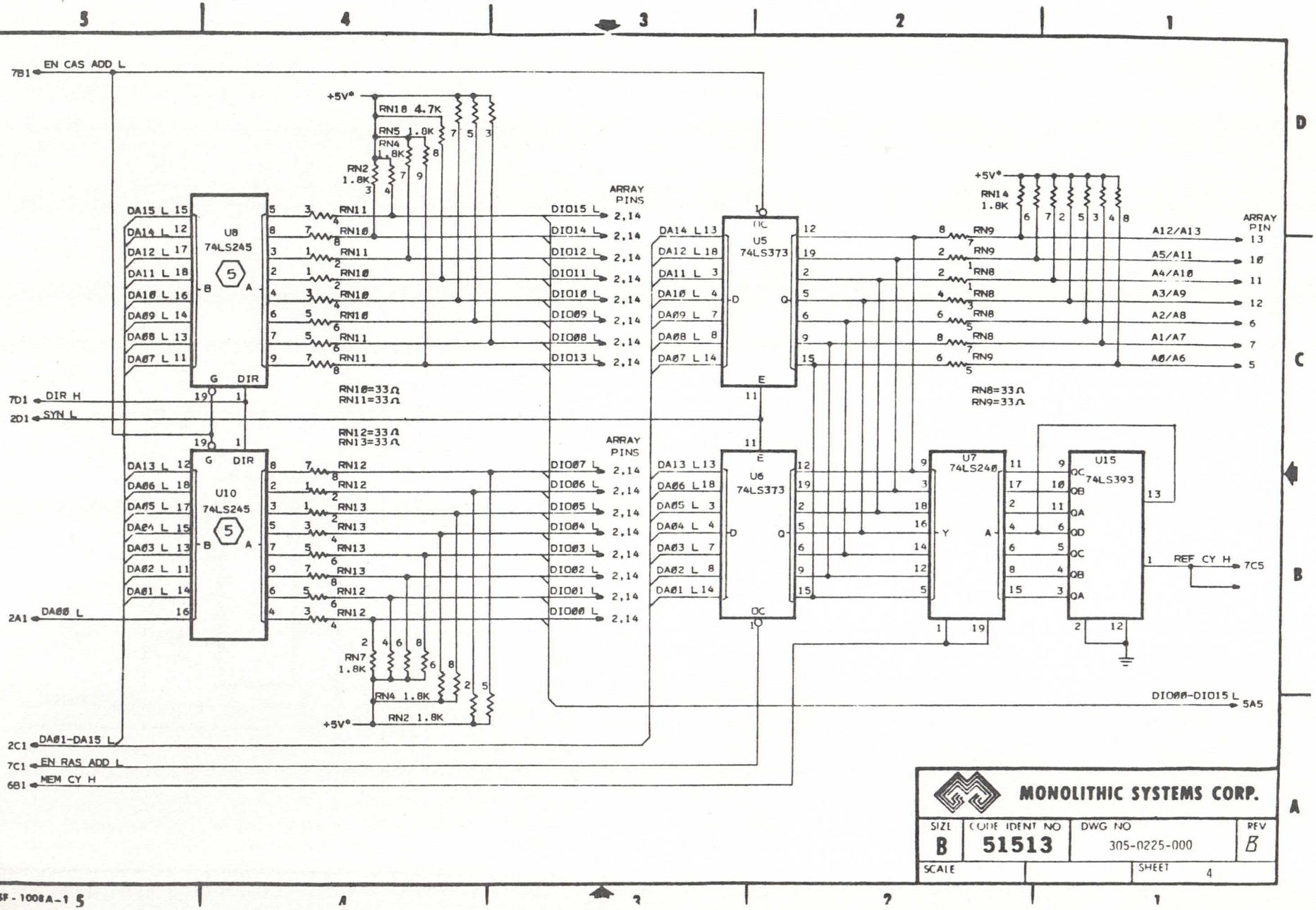
MSF-100RA-1 R


7B1 EN CAS ADD L
+5V*
RN18 4.7K
RN5 1.8K
RN4 1.8K
RN2 1.8K
U8 74LS245
DA15 L 15
DA14 L 12
DA12 L 17
DA11 L 18
DA10 L 16
DA09 L 14
DA08 L 13
DA07 L 11
G DIR
RN11
RN10
DIO15 L
DIO14 L
DIO12 L
DIO11 L
DIO10 L
DIO09 L
DIO08 L
DIO13 L
ARRAY PINS
2,14
7D1 DIR H
2D1 SYN L
RN10=33Ω
RN11=33Ω
RN12=33Ω
RN13=33Ω
U10 74LS245
DA13 L 12
DA06 L 18
DA05 L 17
DA04 L 15
DA03 L 13
DA02 L 11
DA01 L 14
2A1 DA00 L
RN12
RN13
DIO07 L
DIO06 L
DIO05 L
DIO04 L
DIO03 L
DIO02 L
DIO01 L
DIO00 L
RN7 1.8K
RN4 1.8K
RN2 1.8K
+5V*
2C1 DA01-DA15 L
7C1 EN RAS ADD L
6B1 MEM CY H
U5 74LS373
U6 74LS373
DA14 L 13
DA12 L 18
DA11 L 3
DA10 L 4
DA09 L 7
DA08 L 8
DA07 L 14
DA13 L 13
DA06 L 18
DA05 L 3
DA04 L 4
DA03 L 7
DA02 L 8
DA01 L 14
D Q E OC
RN14 1.8K
RN9
RN8
A12/A13
A5/A11
A4/A10
A3/A9
A2/A8
A1/A7
A0/A6
ARRAY PIN
13
10
11
12
6
7
5
RN8=33Ω
RN9=33Ω
U7 74LS240
U15 74LS393
Y A
QC QB QA QD
REF CY H
7C5
DIO00-DIO15 L
5A5
MONOLITHIC SYSTEMS CORP.
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DWG NO 305-0225-000
REV B
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SHEET 4
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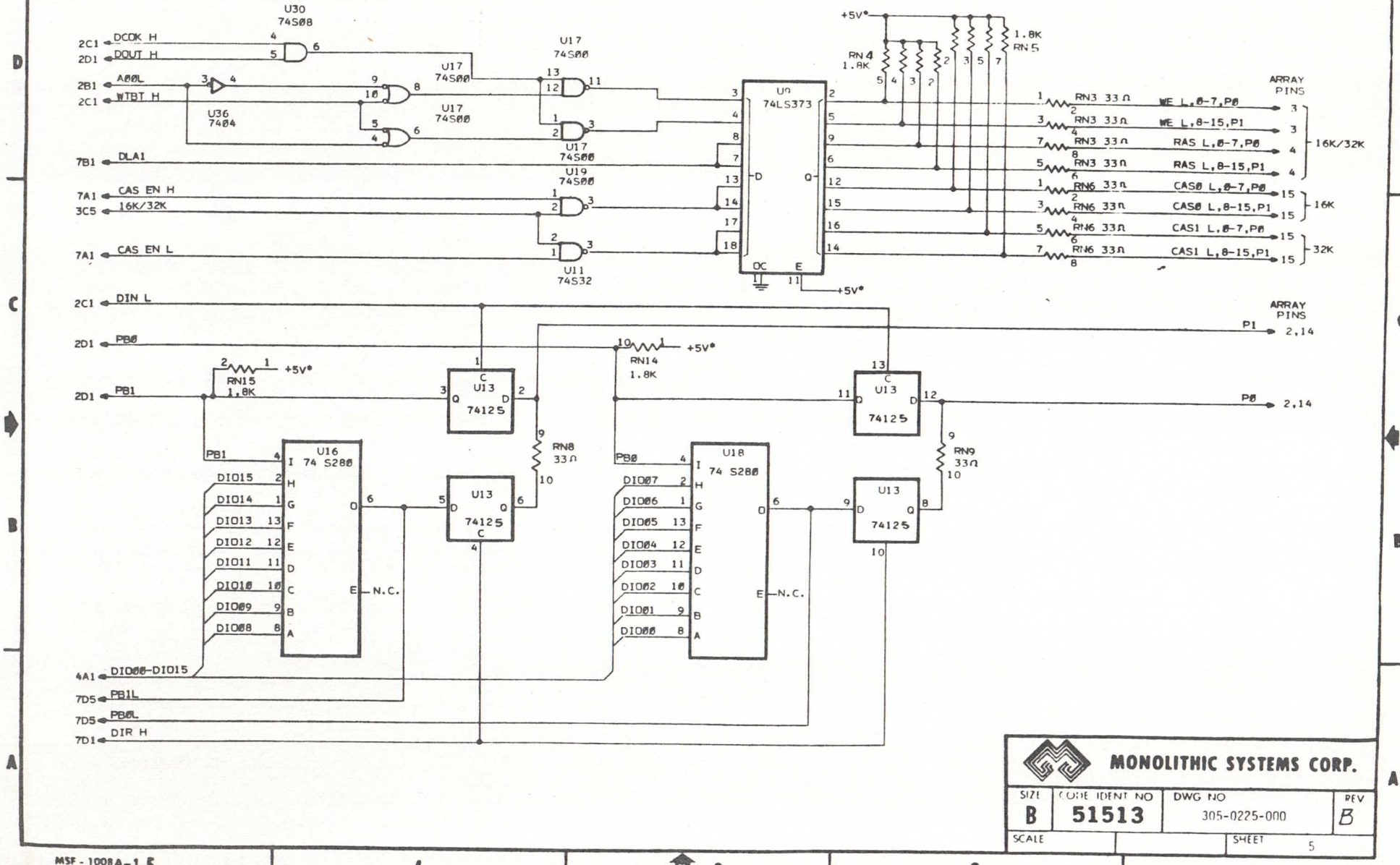

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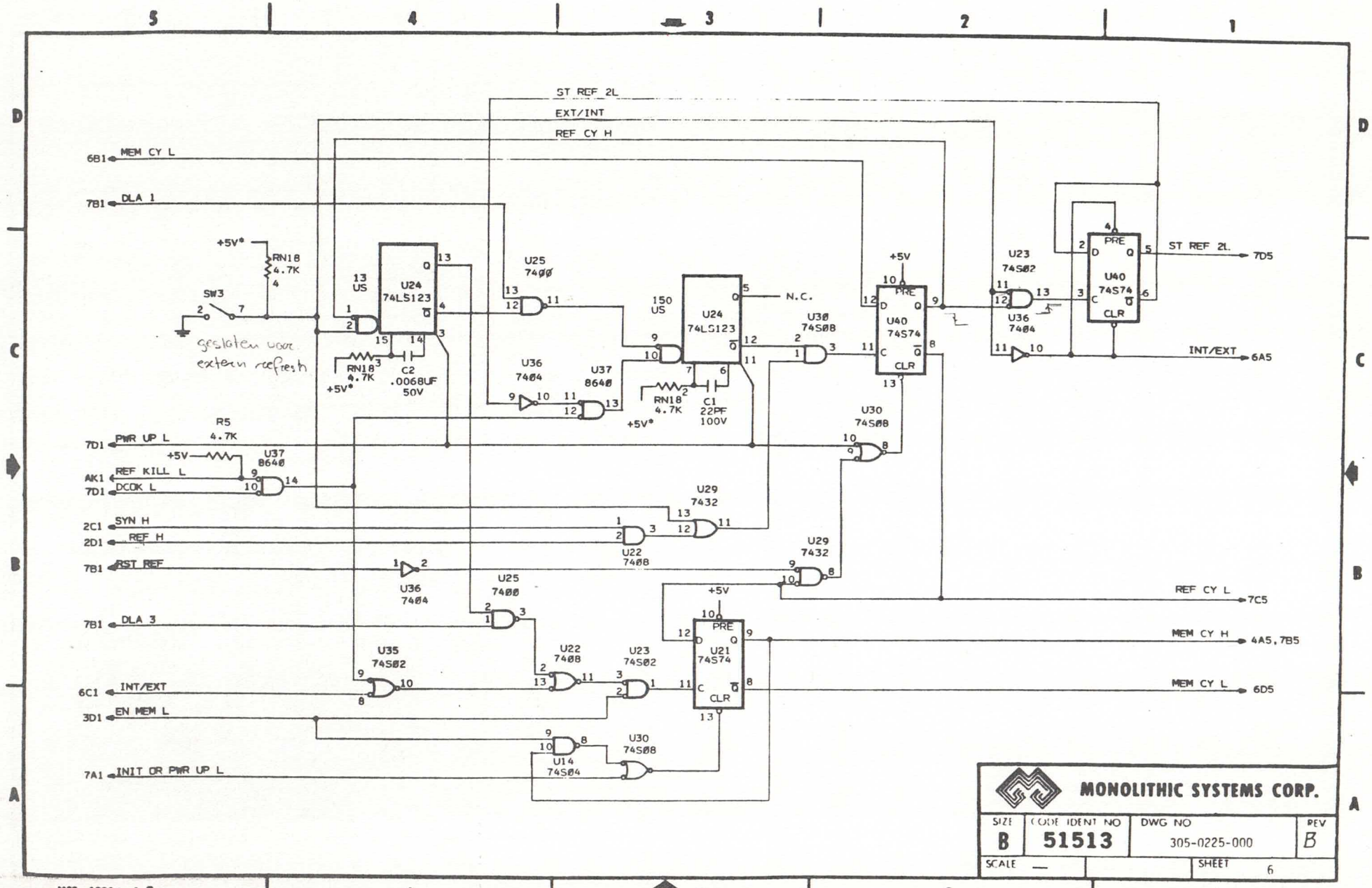
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EXT/INT
REF CY H
6B1 MEM CY L
7B1 DLA 1
+5V*
RN18 4.7K
SW3
13 US
U24 74LS123
U25 74ØØ
150 US
N.C.
U36 7404
U37 8640
U30 74S08
U40 74S74
U23 74S02
ST REF 2L 7D5
INT/EXT 6A5
gesloten voor extern refresh
RN18 4.7K
C2 .0068UF 50V
C1 22PF 100V
R5 4.7K
7D1 PWR UP L
AK1 REF KILL L
7D1 DCOK L
2C1 SYN H
2D1 REF H
U29 7432
U22 74Ø8
7B1 RST REF
REF CY L 7C5
7B1 DLA 3
U35 74S02
MEM CY H 4A5, 7B5
6C1 INT/EXT
MEM CY L 6D5
3D1 EN MEM L
U21 74S74
U14 74S04
7A1 INIT OR PWR UP L
MONOLITHIC SYSTEMS CORP.
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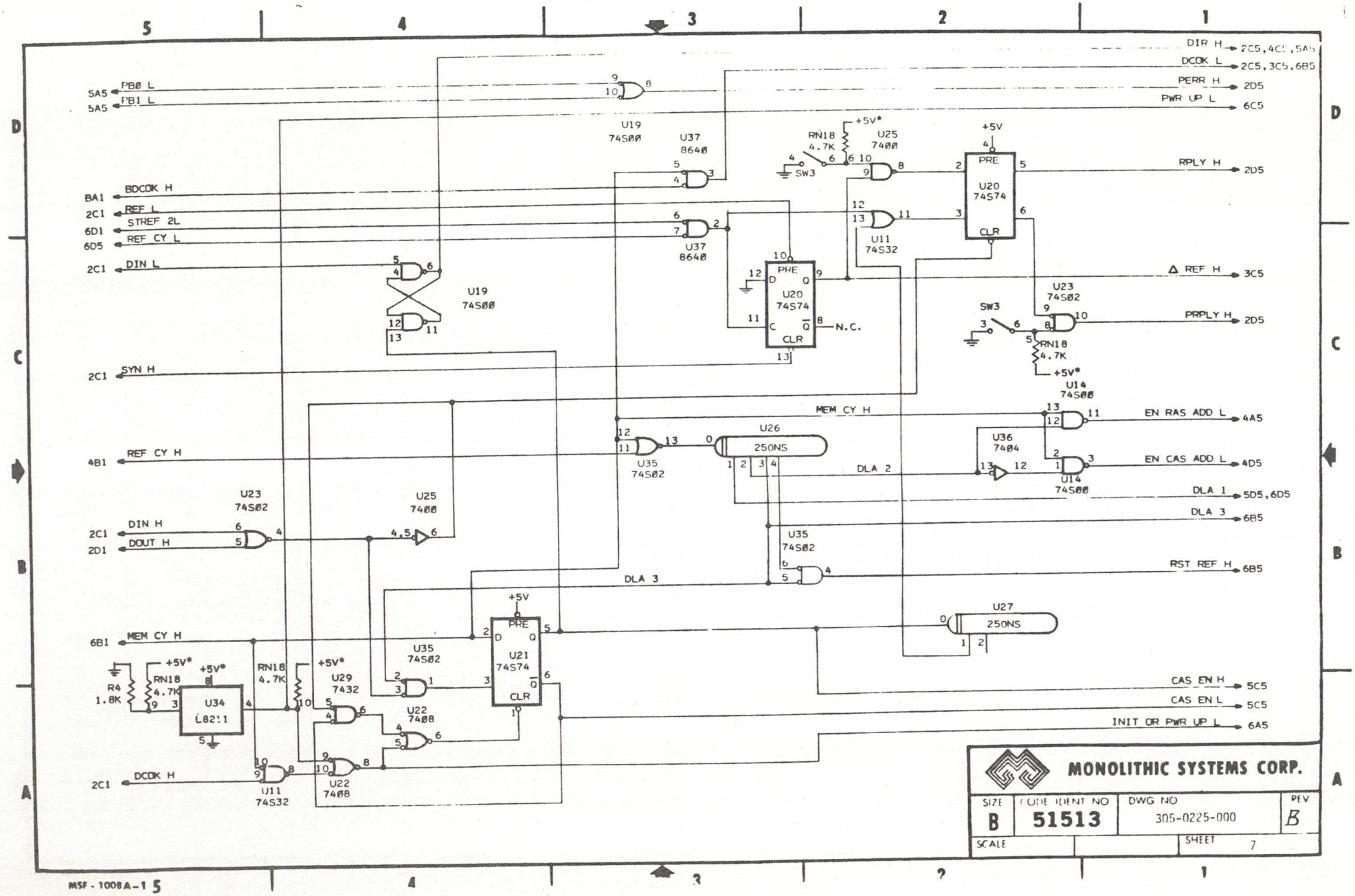
CODE IDENT NO 51513
DWG NO 305-0225-000
REV B
SCALE —
SHEET 6
MSF-1008A-1


DIR H → 2C5,4C5,5A5
DCOK L → 2C5,3C5,6B5
PERR H → 2D5
PWR UP L → 6C5
RPLY H → 2D5
Δ REF H → 3C5
PRPLY H → 2D5
EN RAS ADD L → 4A5
EN CAS ADD L → 4D5
DLA 1 → 5D5,6D5
DLA 3 → 6B5
RST REF H → 6B5
CAS EN H → 5C5
CAS EN L → 5C5
INIT OR PWR UP L → 6A5
5A5 PB0 L
5A5 PB1 L
BA1 BDCOK H
2C1 REF L
6D1 STREF 2L
6D5 REF CY L
2C1 DIN L
2C1 SYN H
4B1 REF CY H
2C1 DIN H
2D1 DOUT H
6B1 MEM CY H
2C1 DCOK H
MEM CY H
DLA 2
DLA 3
U19 74S00
U37 8640
U25 7400
U20 74S74
U11 74S32
U23 74S02
U14 74S00
U36 7404
U26 250NS
U27 250NS
U35 74S02
U21 74S74
U29 7432
U22 7408
U34 L8211
RN18 4.7K
R4 1.8K
SW3
+5V
+5V*
N.C.
MONOLITHIC SYSTEMS CORP.
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DWG NO 305-0225-000
REV B
SCALE
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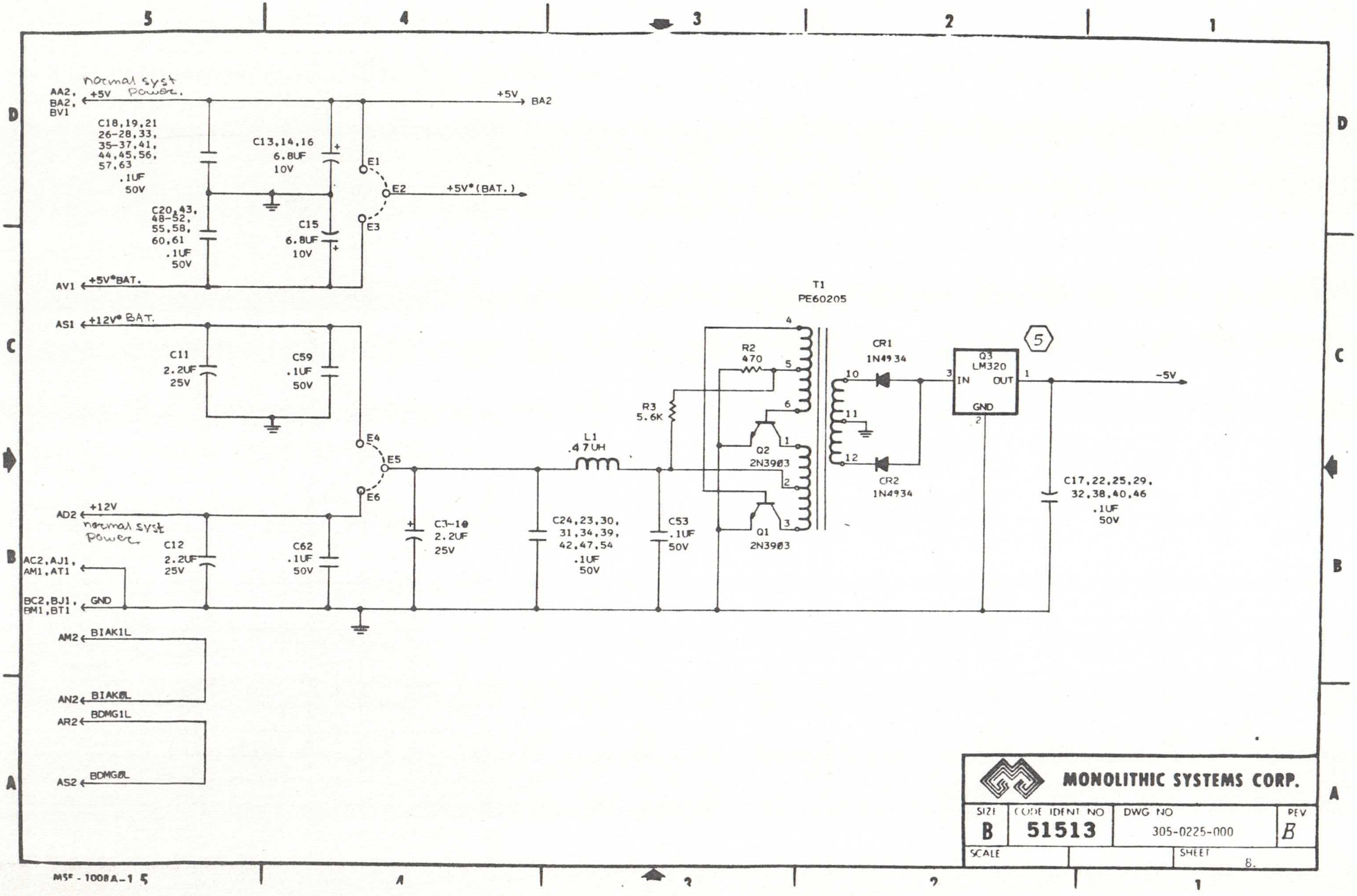
MSF-1008A-1



MONOLITHIC SYSTEMS CORP.			
SIZE B	CODE IDENT NO 51513	DWG NO 305-0225-000	REV B
SCALE		SHEET 8.	

MSC - 1008A-1

DEVICE TYPE NO.	REFERENCE DESIGNATION	NOTE	POWER & GROUND							REMARKS/SPARES	LINE NO.
			GND	+5V							
I.C. 7400	U25		7	14							1
I.C. 74S00	U14,17,19		7	14						U19:4,5,6/11,12,13	2
I.C. 74S02	U23,35		7	14							3
I.C. 7404	U28,36		7	14							4
I.C. 7408	U22		7	14							5
I.C. 74S08	U30		7	14							6
I.C. 7432	U29		7	14							7
I.C. 74S32	U11		7	14							8
I.C. 7439	U39										9
I.C. 74S74	U20,U21,U40		7	14							10
I.C. 7483A	U1,2,3,12		12	5							11
I.C. 74LS123	U24		8	16							12
I.C. 74LS240	U7,U38		10	20							13
			10	20							14
I.C. 74LS280	U16,U18		7	14							15
I.C. 74LS373	U4,5,6,9		10	20							16
I.C. 74LS393	U15		7	14							17
I.C. 74125	U13		7	14							18
I.C. L8211	U34										19
I.C. 8640	U37										20
I.C. 74S04	U31										21
I.C. 74LS245	U8,U10,U32,U33		10	20							22
I.C. 74LS645			10	20							23

DEVICE TYPE NO.	REFERENCE DESIGNATION	NOTE	POWER & GROUND							REMARKS/SPARES	LINE NO.
			GND	+5V							

MONOLITHIC SYSTEMS CORP.

SIZE	CODE IDENT NO	DWG NO	REV
B	51513	305-0225-000	B

SCALE | SHEET 9